# Beware of Hand Calculations for Short Circuit Studies

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AUTHOR: John Merrell

## INTRODUCTION

In a recent short circuit study performed by Power Systems Engineering, a question was raised concerning the fallacy of using simple hand calculations. The details of this problem will be discussed below. But to begin, please notice the one-line diagram shown in Figure 1 below. In this one-line, PSE 1 and PSE 2 are utility services and are modeled identically. Generators GEN 1, 2, and 3 are all identical to each other.

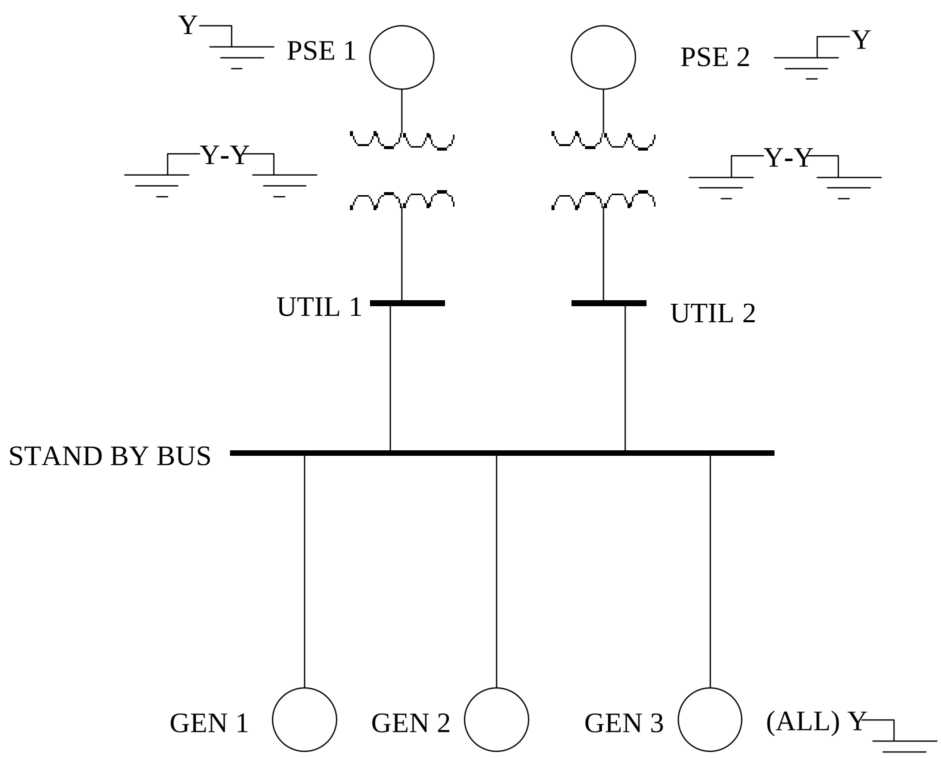


**Figure 1. One-line diagram of the system in question.**

In the course of this study, the network in Figure 1 was broken apart. Each source was considered separately; that is, all other sources were disconnected. Fault current for SLG and three-phase faults were calculated at the STAND BY BUS for each source alone. The sum of these fault currents was then compared to the fault current of the network with all sources contributing.

First, the utility services were disconnected from the STAND BY BUS. For both fault types, the fault current produced by all three generators was found to be approximately triple that for a single generator with the other two off line.

Next, all generators were taken off line. The STAND BY BUS was then fed only by utility power. The fault current with both utility sources contributing was found to be approximately double that of only one utility source.

With all sources contributing fault current to the STAND BY BUS, the fault current for a three-phase fault was equal to the sum of three-phase fault currents found above. However, the actual true SLG fault current with all sources contributing was *greater* than the sum of SLG fault current from each source considered alone.

Why does the fault current for a SLG fault type become greater than the sum of fault currents from each source considered independently? The purpose of this article is to investigate why this occurs by constructing sequence networks and calculating fault currents accordingly. Then, conclusions will be drawn from the analysis. The significance of such an investigation is this: the design engineer cannot reply upon using simple calculations and patterns. Rigorous mathematical analysis or computer simulation is safest for professional design work.

## ANALYSIS

Table 1 below summarizes the generator, conductor, and transformer impedances, all in per unit, for each sequence. The kVA base is 10,000, and the kV base is 12.47 for the primary and 0.480 for the secondary.

**Table 1. System impedances in per unit.**

| | Transformers | | | | | |
|---|---|---|---|---|---|---|
| | $R^0$ | $R^-$ | $R^+$ | $X^0$ | $X^-$ | $X^+$ |
| **PSE 1 to UTIL 1** | 3.88E-02 | 3.88E-02 | 3.88E-02 | 2.62E-01 | 2.62E-01 | 2.62E-01 |
| **PSE 2 to UTIL 2** | 3.88E-02 | 3.88E-02 | 3.88E-02 | 2.62E-01 | 2.62E-01 | 2.62E-01 |
| | **Generators and Utility Service** | | | | | |
| | $R^0$ | $R^-$ | $R^+$ | $X^0$ | $X^-$ | $X^+$ |
| **PSE 1** | 2.02E-04 | 2.02E-04 | 2.02E-04 | 1.01E-03 | 1.01E-03 | 1.01E-03 |
| **PSE 2** | 2.02E-04 | 2.02E-04 | 2.02E-04 | 1.01E-03 | 1.01E-03 | 1.01E-03 |
| **GEN 1** | 3.48E-02 | 3.48E-02 | 3.48E-02 | 2.19E-02 | 9.83E-01 | 1.02 |
| **GEN 2** | 3.48E-02 | 3.48E-02 | 3.48E-02 | 2.19E-02 | 9.83E-01 | 1.02 |
| **GEN 3** | 3.48E-02 | 3.48E-02 | 3.48E-02 | 2.19E-02 | 9.83E-01 | 1.02 |
| | **Conductors** | | | | | |
| | $R^0$ | $R^-$ | $R^+$ | $X^0$ | $X^-$ | $X^+$ |
| **UTIL 1 to UTIL 2** | 2.41E-02 | 1.08E-03 | 1.08E-03 | 2.40E-03 | 1.07E-03 | 1.07E-03 |
| **UTIL 1 to STAND BY BUS** | 2.41E-02 | 1.08E-03 | 1.08E-03 | 2.40E-03 | 1.07E-03 | 1.07E-03 |
| **UTIL 2 to STAND BY BUS** | 2.41E-02 | 1.08E-03 | 1.08E-03 | 2.40E-03 | 1.07E-03 | 1.07E-03 |
| **GEN 1 to STAND BY BUS** | 2.03E-02 | 5.86E-03 | 5.86E-03 | 2.07E-02 | 1.04E-02 | 1.04E-02 |
| **GEN 2 to STAND BY BUS** | 3.41E-02 | 9.84E-03 | 9.84E-03 | 3.48E-02 | 1.74E-02 | 1.74E-02 |
| **GEN 3 to STAND BY BUS** | 4.18E-02 | 1.21E-02 | 1.21E-02 | 4.27E-02 | 2.13E-02 | 2.13E-02 |

To find three-phase faults at the "STAND BY BUS," we must first find the pre-fault voltage (usually assumed to be nominal) and then find the equivalent positive-sequence impedance of the network as seen from the faulted bus. The three-phase fault current is found by taking the pre-fault voltage and dividing by the magnitude of the equivalent positive-sequence impedance. Figure 2 below shows the circuit used in finding the equivalent positive-sequence impedance for both the three-phase and SLG fault analyses.

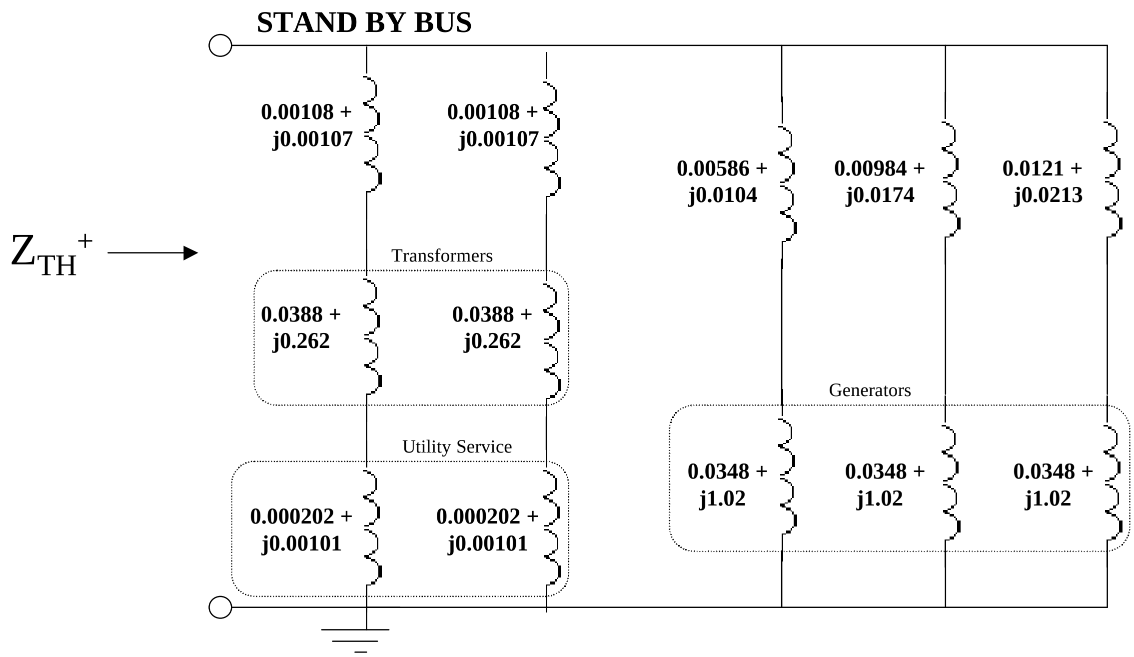


**Figure 2. Circuit used to calculate equivalent positive-sequence impedance.**

The positive-sequence impedance is

$$
\begin{aligned}
Z_{TH}^{+} &= \left[\frac{(0.00108 + j0.00107) + 3(0.0388 + j0.262) + 3(0.000202 + j0.00101)}{3}\right] \| \\
&\quad [(0.00586 + j0.0104) + (0.0348 + j1.02)] \| [(0.00984 + j0.0174) + (0.0348 + j1.02)] \| \\
&\quad [(0.0121 + j0.0213) + (0.0348 + j1.02)] \\
&= 0.0116 + j0.0957
\end{aligned}
$$

The three-phase fault current is then

$$
\begin{aligned}
I_{af}^{3f} &= \left[\frac{V_{an}^{pf}}{Z_{TH}^{+}}\right]\left[\frac{S_B^{3f}}{V_B^{l-l}\sqrt{3}}\right] \\
&= \left[\frac{1 p.u.}{0.0116 + j0.0957}\right]\left[\frac{10{,}000}{0.480\sqrt{3}}\right] \\
&= 124.8 kA \angle -83.09^{\circ}.
\end{aligned}
$$

Here $V_{an}^{pf}$ is the pre-fault voltage at the STAND BY BUS and $I_{af}^{3f}$ is the three-phase fault current.

In calculating SLG fault current, the equivalent negative and zero-sequence impedances as seen from the faulted bus must be found. Figure 3 below shows the circuits used to find these impedances.

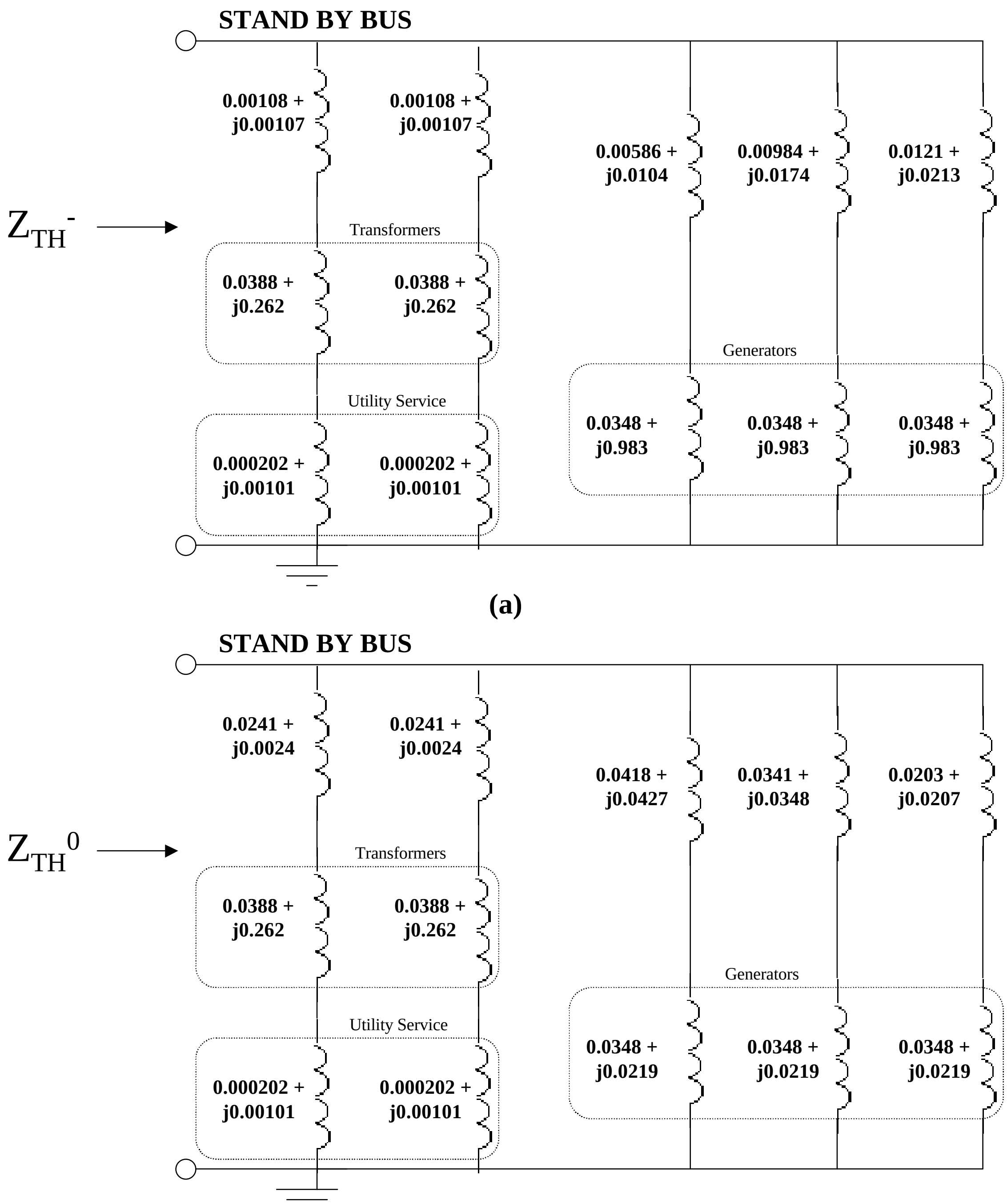


**Figure 3. Circuit used to calculate equivalent (a) negative-sequence and (b) zero-sequence impedances.**

The equivalent negative and zero-sequence impedances, respectively, are

$$Z_{TH}^{-} = \left[\frac{(0.00108 + j0.00107) + 3(0.0388 + j0.262) + 3(0.000202 + j0.00101)}{3}\right] \|$$
$$\left[(0.00586 + j0.0104) + (0.0348 + j0.983)\right] \| \left[(0.00984 + j0.0174) + (0.0348 + j0.983)\right] \|$$

$$\left[(0.0121 + j0.0213) + (0.0348 + j0.983)\right]$$
$$= 0.0114 + j0.0947$$

$$Z_{TH}^{0} = \left[\frac{(0.0241 + j0.0024) + 3(0.0388 + j0.262) + 3(0.000202 + j0.00101)}{3}\right] \|$$
$$\left[(0.0418 + j0.0427) + (0.0348 + j0.0219)\right] \| \left[(0.0341 + j0.0348) + (0.0348 + j0.0219)\right] \|$$
$$\left[(0.0203 + j0.0207) + (0.0348 + j0.0219)\right]$$
$$= 0.017 + j0.017$$

To find SLG fault current, the circuit shown in Figure 4 must be constructed. Here, $V_{an}^{pf}$ is the pre-fault voltage at the faulted bus. $Z_{TH}^{+}$, $Z_{TH}^{-}$, and $Z_{TH}^{0}$ are the positive, negative, and zero-sequence impedances, respectively.

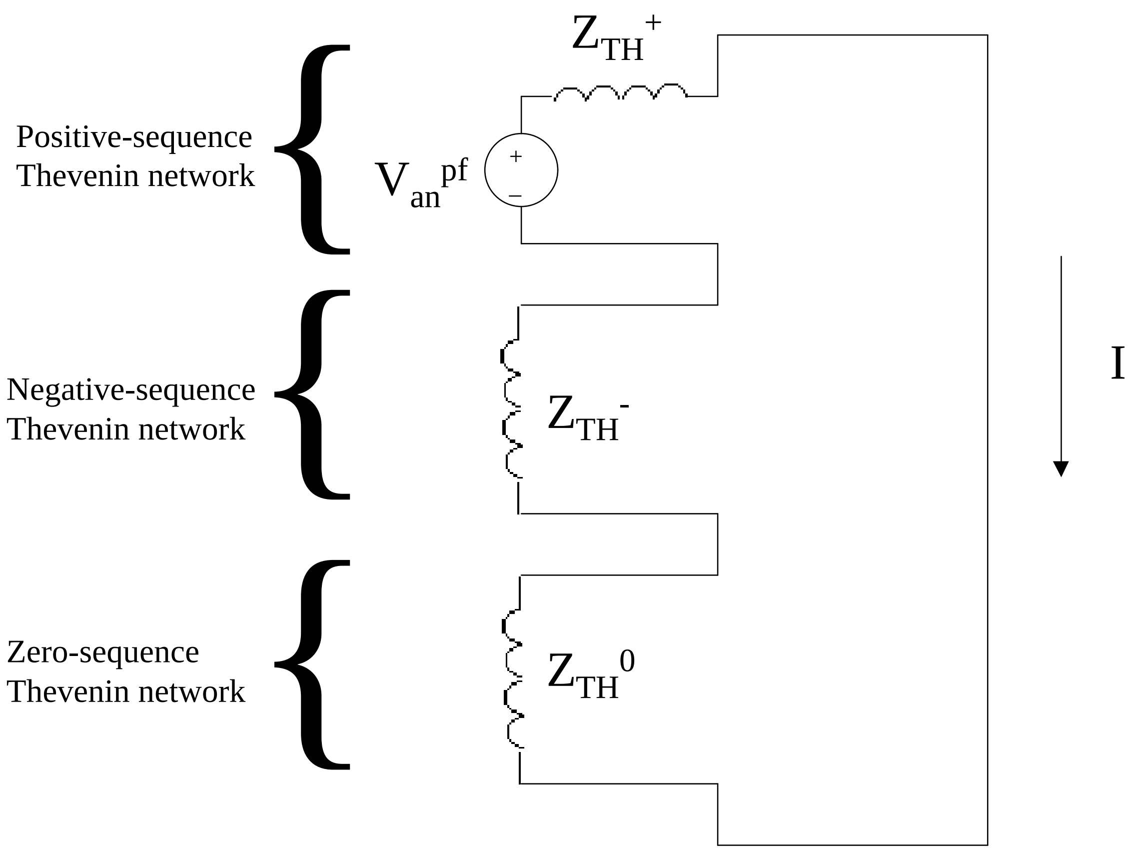


**Figure 4. General circuit used to calculate SLG fault current.**

The fault current ($I_{af}^{SLG}$) is three times the current $I$ in Figure 4 (i.e., $I_{af}^{SLG} = 3I$). The SLG fault current is then

$$I_{af}^{SLG} = \left[\frac{3V_{an}^{pf}}{Z_{TH}^{+} + Z_{TH}^{-} + Z_{TH}^{0}}\right]\left[\frac{S_B^{3f}}{V_B^{l-l}\sqrt{3}}\right]$$

$$= \left[ \frac{3(1p.u.)}{(0.0116 + j0.0957) + (0.0114 + j0.0947) + (0.017 + j0.017)} \right] \left[ \frac{10{,}000}{0.480\sqrt{3}} \right]$$
$$= 171kA\angle -79.1^{\circ}$$

**RESULTS**

Remember that the issue at hand is this: for a SLG fault, why is the fault current at the STAND BY BUS shown in Figure 1 larger than the sum of the fault currents from each source considered separately? Notice that in Figure 1, all sources are in parallel as seen by the STAND BY BUS. Because three-phase faults are only positive-sequence, the fault current can be calculated by taking each parallel branch, finding the fault current contribution (pre-fault voltage divided by positive-sequence impedance), and then adding up the fault contributions. This explains why there was an additive effect for three-phase faults.

For an SLG fault, all sequences must be considered. The positive-sequence impedances of each parallel branch (as seen by the STAND BY BUS) must be placed in parallel. The same is true for the negative and zero-sequences. *These parallel combinations must then be placed in series.* This topology is illustrated in Figure 5(b).

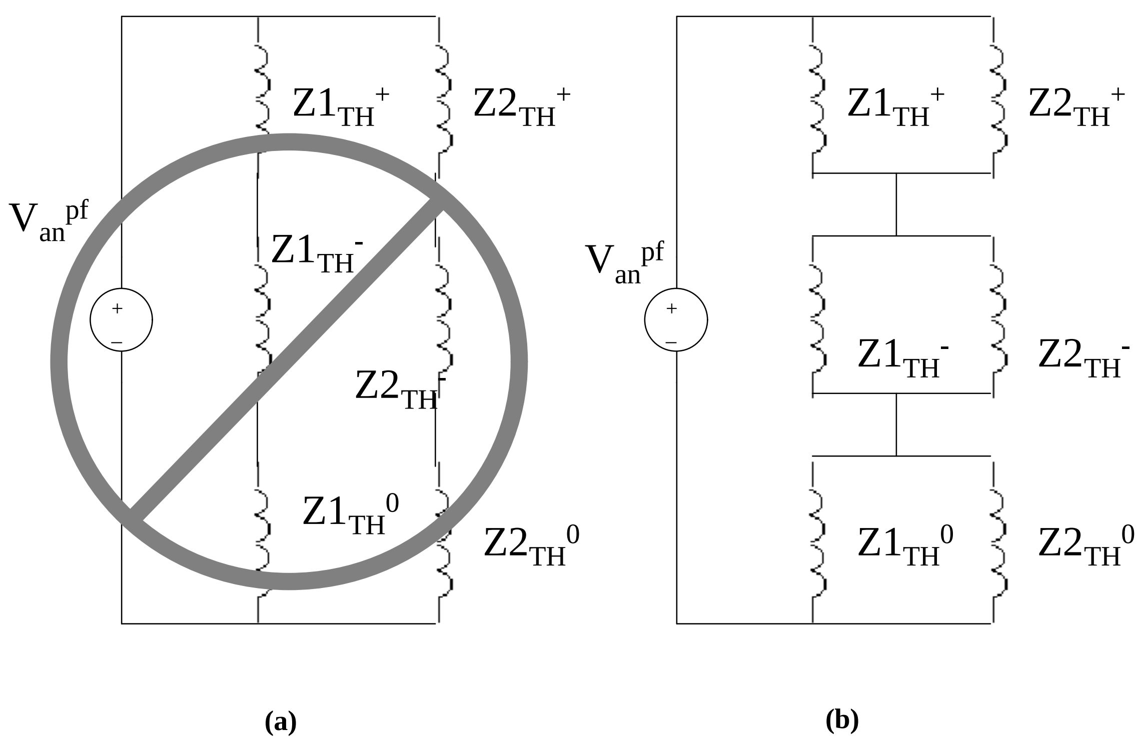


**Figure 5. (a) Incorrect and (b) correct combination for parallel systems 1 and 2 for SLG fault types.**

The fallacy in assuming that the fault currents from each source considered separately can be added to produce the total fault current probably results from assuming a topology like that shown in Figure 5(a). In general, these two topologies are not equivalent. In fact, the equivalent impedance for Figure 5(b) can be lower than that in Figure 5(a). Lower impedance leads to higher fault current.

Table 2 below compares the sum of fault currents from each source considered separately, the fault current as calculated above, and the fault current produced by the EDSA software package.

**Table 2. Comparison of methods.**

| | SLG Fault (kA) | Three-Phase Fault (kA) |
|---|---|---|
| **GEN 1 Only** | 17 | 12 |
| **GEN 2 Only** | 17 | 12 |
| **GEN 3 Only** | 17 | 12 |
| **PSE 1 Only** | 45 | 45 |
| **PSE 2 Only** | 45 | 45 |
| **Sum =** | 141 | 126 |
| **Detailed Hand Calc.** | 171 | 125 |
| **EDSA Result** | 171 | 125 |

Note that for the SLG, there is a sizable difference between the fault current from hand calculations/EDSA results and the sum of fault currents from individual sources. The three-phase fault currents, however, are essentially equal. There is a small difference, probably due to rounding.

## CONCLUSION

In this article, the effect upon fault current of adding parallel systems to a faulted bus was investigated. Because of the way in which the equivalent sequence impedances are connected for a SLG fault as opposed to a three-phase fault, the SLG fault current for a system can be larger than the sum of the fault currents for sources considered alone. Under certain circumstances the fault current will equal the sum of fault currents from contributing sources considered separately, but not in general. Therefore, the design engineer should take care when using simple calculations. Rather, the engineer should resort to either a thorough hand calculation or a computer simulation to perform the analysis.

## ABOUT THE AUTHOR:

John Merrell is an electrical engineer at Power Systems Engineering, P.S.. He is responsible for performing short circuit, harmonic, load flow, and protection device coordination studies for industrial, commercial, and utility clients. Based in outside of Seattle, Washington since 1986, Power Systems Engineering is an electrical engineering consulting firm specializing in power systems studies, power quality, and commissioning services. Customers include Boeing, University of Washington, General Electric, Siemens, Square D, Cutler-Hammer, and many others. Their web page address is www.powerstudies.com.